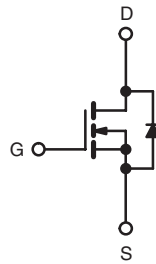
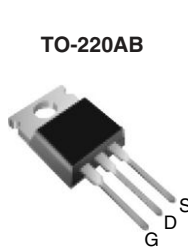


Power MOSFET

PRODUCT SUMMARY		
V_{DS} at T_J max. (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.190
Q_g (Max.) (nC)	98	
Q_{gs} (nC)	17	
Q_{gd} (nC)	25	
Configuration	Single	

FEATURES

- High E_{AR} Capability
- Lower Figure-of-Merit $R_{on} \times Q_g$
- 100 % Avalanche Tested
- High Peak Current Capability
- dV/dt Ruggedness
- Effective C_{OSS} Specified
- Improved Transconductance
- Improved t_{rr}/Q_{rr}
- Improved Gate Charge
- High Power Dissipation Capability
- Compliant to RoHS Directive 2002/95/EC



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP22N60S-E3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V_{DS}		600	V	
Gate-Source Voltage	V_{GS}		± 20		
Continuous Drain Current ^a	V_{GS} at 10 V	$T_C = 25$ °C	22	A	
		$T_C = 100$ °C	13		
Pulsed Drain Current ^b	I_{DM}		65		
Linear Derating Factor	TO-220AB		2	W/°C	
Single Pulse Avalanche Energy ^c	E_{AS}		690	mJ	
Repetitive Avalanche Energy ^b	E_{AR}		25		
Maximum Power Dissipation	TO-220AB		P_D	250	W
Peak Diode Recovery dV/dt ^d	dV/dt		7.3	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) ^e	for 10 s		300		

Notes


- Limited by maximum junction temperature.
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- $I_{SD} \leq 22$ A, $dI/dt \leq 340$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	TO-220AB	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	TO-220AB	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}$	-	0.160	0.190	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 13\text{ A}$		-	9.4	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$		-	2810	-	pF
Output Capacitance	C_{oss}			-	1480	-	
Reverse Transfer Capacitance	C_{rss}			-	33	-	
Effective Output Capacitance (Time Related)	$C_{oss\text{ eff. (TR)}}^a$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	155	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}, V_{DS} = 480\text{ V}$	-	75	-	nC
Gate-Source Charge	Q_{gs}			-	17	-	
Gate-Drain Charge	Q_{gd}			-	25	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 22\text{ A},$ $R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$		-	24	-	ns
Rise Time	t_r			-	68	-	
Turn-Off Delay Time	$t_{d(off)}$			-	77	-	
Fall Time	t_f			-	59	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$		-	0.65	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	22	A
Pulsed Diode Forward Current	I_{SM}			-	-	88	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 22\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}, I_F = I_S,$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	462	-	ns
Reverse Recovery Charge	Q_{rr}			-	8.3	-	μC
Reverse Recovery Current	I_{RRM}			-	30	-	A

Note

a. $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

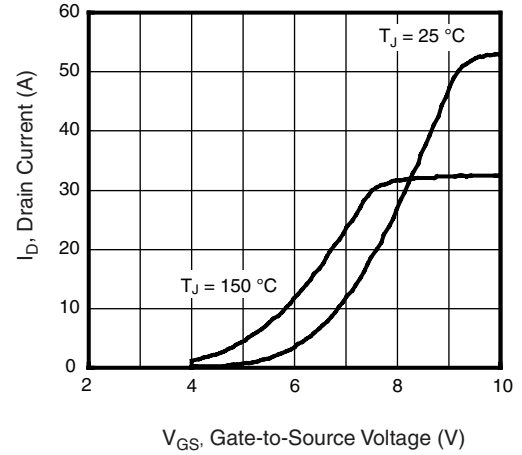
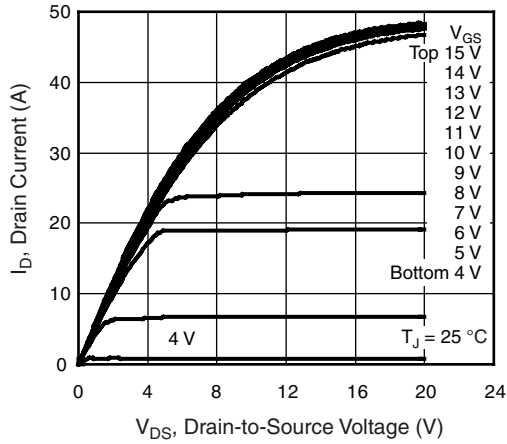


Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

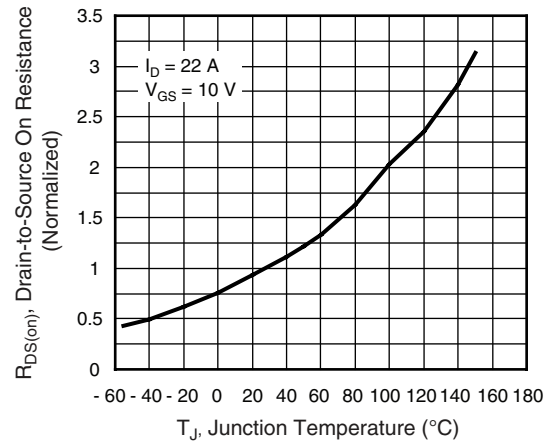
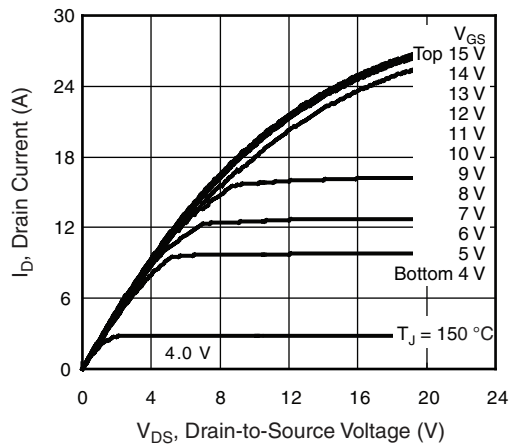


Fig. 2 - Typical Output Characteristics, $T_J = 150\text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

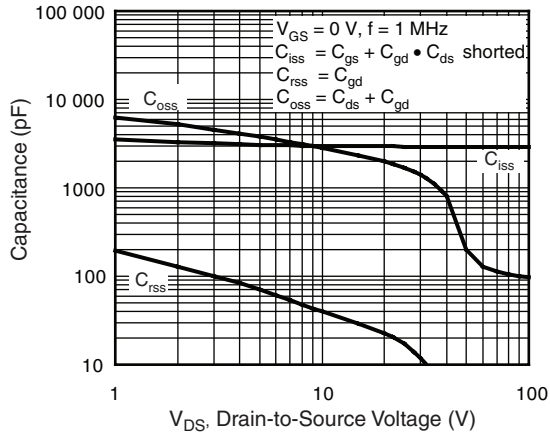


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

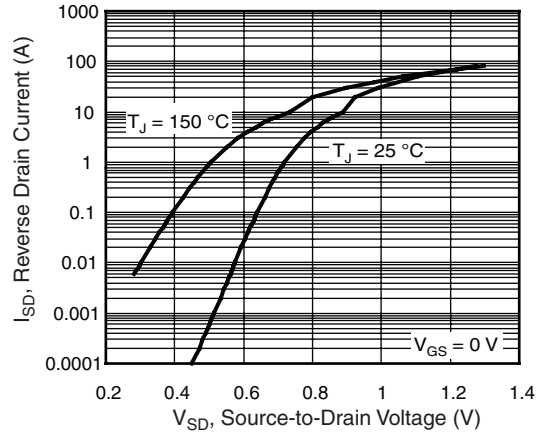


Fig. 7 - Typical Source-Drain Diode Forward Voltage

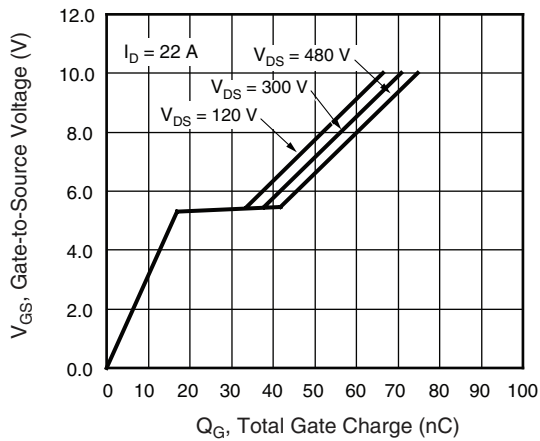


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

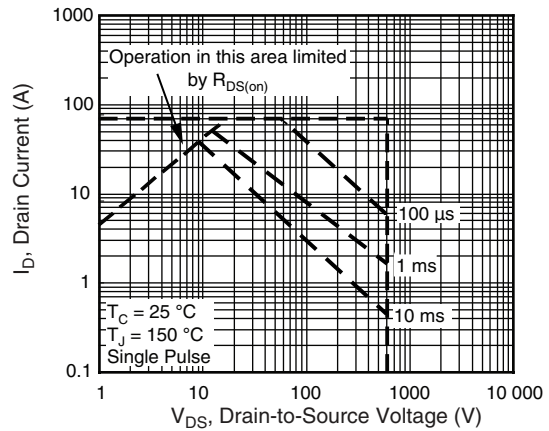


Fig. 8 - Maximum Safe Operating Area

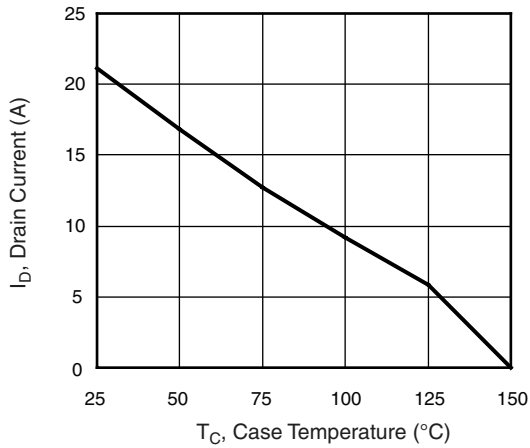


Fig. 9 - Maximum Drain Current vs. Case Temperature

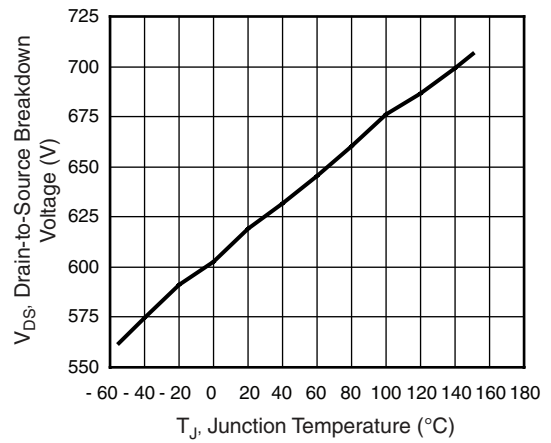


Fig. 10 - Drain-to-Source Breakdown Voltage

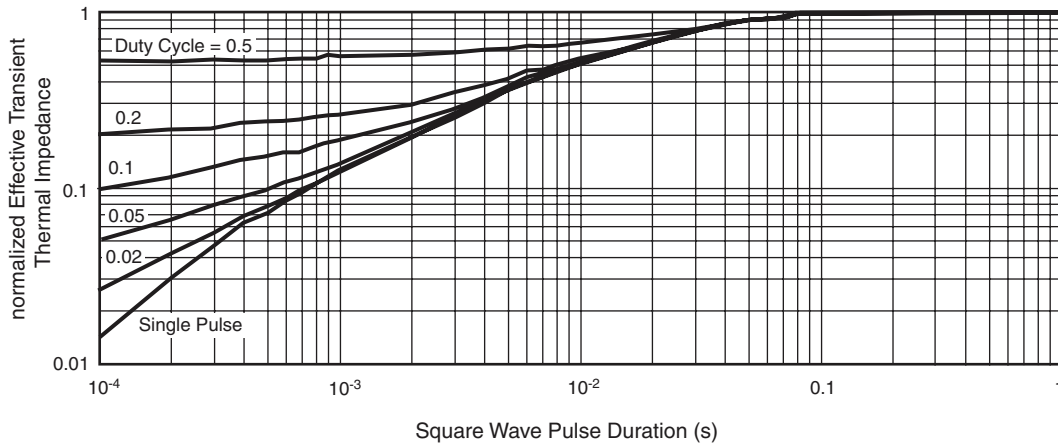


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

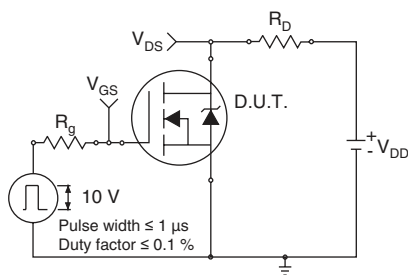


Fig. 11a - Switching Time Test Circuit

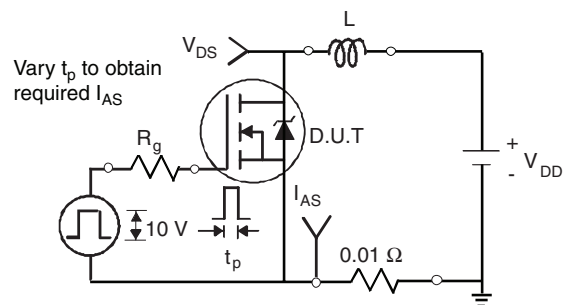


Fig. 12a - Unclamped Inductive Test Circuit

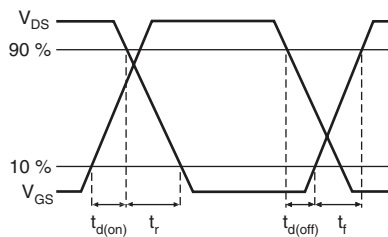


Fig. 11b - Switching Time Waveforms

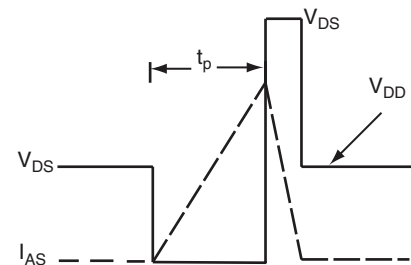


Fig. 12b - Unclamped Inductive Waveforms

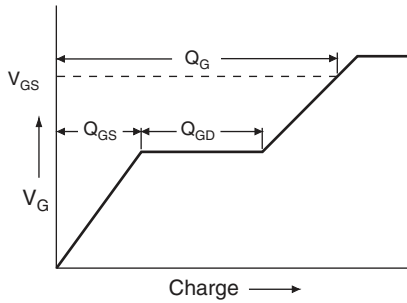


Fig. 13a - Basic Gate Charge Waveform

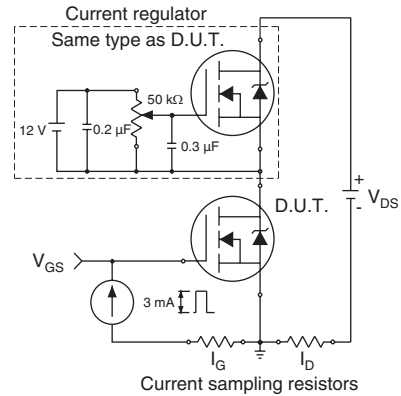
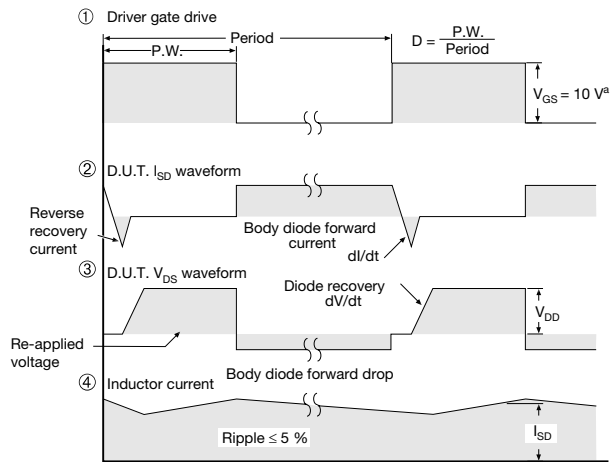
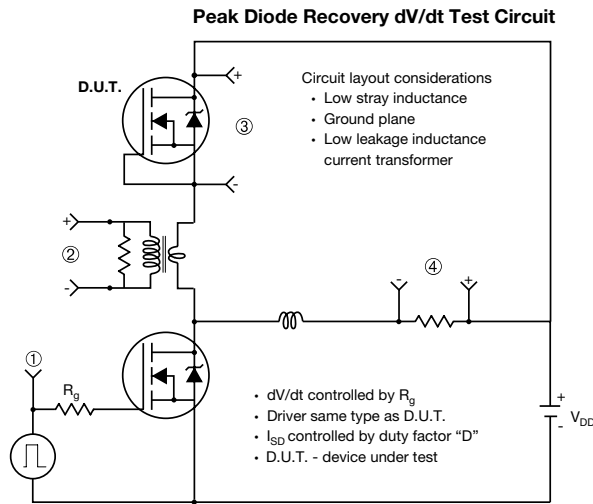


Fig. 13b - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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